REMARKS

In the non-final June 7, 2006 Office Action, the Examiner rejected Claims 1-20. By this Response, Applicants cancel claims 4 and 9-16, amend Claims 1-3, 6, 17, and 20, and add claims 21-25 to clarify Applicants' claimed invention. No new matter is believed introduced by the amendments or new claims.

After entry of this Response, Claims 1-3, 5-8, and 17-25 are pending in the Application. Applicants respectfully assert that Claims 1-3, 5-8, and 17-25 are in condition for allowance and respectfully request reconsideration of the claims in light of the following remarks.

I. Pending Claims

Claim Rejections under 35 U.S.C. § 102(b) and (e)

Claims 1-16 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Harari et al (U.S. Patent No. 5,369,615). Claims 1-7, 9-13, and 15 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Bautista et al (U.S. Patent No.6,891,752). Applicant respectfully traverses this rejection. Applicant respectfully traverses these rejections.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, "[t]he identical invention must be shown in as complete detail as is contained in the * * * claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 1

As amended, claim 1 recites an apparatus, comprising: a memory device including a block of memory operable to store data, said memory device being adapted to at least partially erase said block of memory in a first erase cycle and in a second erase cycle subsequent to the first erase cycle, said memory device being further adapted to store a first voltage increment threshold count and a second voltage increment threshold count associated with said block of memory, said memory device being further adapted to count a total number of erase pulses applied to said block of memory, said memory device being further adapted to apply an erase

pulse to said block of memory during the first and the second erase cycles having an erase pulse voltage level based at least in part on the total number of erase pluses applied to said block of memory, the first voltage increment threshold count, and a second voltage increment threshold count.

Harari does not teach or disclose all of the elements of claim 1. More specifically, Harari does not teach or disclose a memory device adapted to store a first voltage increment threshold count and a second voltage increment threshold count associated with said block of memory or adapted to apply an erase pulse to said block of memory during the first and the second erase cycles having an erase pulse voltage level based at least in part on the total number of erase pluses applied to said block of memory, the first voltage increment threshold count, and a second voltage increment threshold count. Rather, Harari discloses an erase algorithm that accomplishes erasing of a group of memory cells by application of incremental erase pulses, which includes increasing the voltage of an erase pulse once an erase function fails to erase a memory block. Harari does not disclose repeatedly applying an erase pulse with the same voltage a number of times and keeping count of the number of pulses applied. Furthermore, Harari does not disclose a first and a second voltage increment threshold count used to determine if the erase pulse voltage should be increased. Therefore, Harari does not teach or disclose all of the elements of claim 1.

Bautista does not teach or disclose all of the elements of claim 1. More specifically, Bautista does not teach or disclose a memory device adapted to store a first voltage increment threshold count and a second voltage increment threshold count associated with said block of memory or adapted to apply an erase pulse to said block of memory during the first and the second erase cycles having an erase pulse voltage level based at least in part on the total number of erase pulses applied to said block of memory, the first voltage increment threshold count, and a second voltage increment threshold count. Rather, Bautista discloses method for erase voltage control where an erase voltage is applied to the set of memory cells and if the set of memory cells is not fully erased the erase voltage is ramped. Bautista further discloses that the gate erase voltage may be increased as a matter of course, or the voltage may be increased only if a certain number of pulses have been applied at the present voltage. Bautista does not disclose counting the total number of erase pulses applied to the memory block nor does Bautista disclose maintaining both a first voltage increment threshold count and a second voltage increment

threshold count. Therefore, Bautista does not teach or disclose all of the elements of claim 1.

Claims 2, 3, and 5-8

Claims 2, 3, and 5-8 variously depend from claim 1 and are believed to be allowable due at least to their dependency.

Claim Rejection under 35 U.S.C. § 103(a)

Claims 17- 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Harari et al (U.S. Patent No. 5,369,615) in view of Harari et. Al (U.S. Patent No. 5,297,148). For an obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970).

Claim 17

As amended, claim 17 recites an apparatus, comprising: a first block of memory operable to store data and to be at least partially erased in a first erase cycle and in a second erase cycle subsequent to the first erase cycle; a first memory location uniquely associated with said first block of memory, said first memory location being adapted to store an initial erase pulse voltage level for an erase pulse to be applied to said first block of memory during the second erase cycle, and said first memory location being adapted to store a first voltage increment threshold count and a second voltage increment threshold count associated with said first block of memory; a second block of memory operable to store data and to be at least partially erased in a first erase cycle and in a second erase cycle subsequent to the first erase cycle; a second memory location uniquely associated with said second block of memory, said second memory location being adapted to store an initial erase pulse voltage level for an erase pulse to be applied to said second block of memory during the second erase cycle, and said second memory location being adapted

to store a first voltage increment threshold count and a second voltage increment threshold count associated with said second block of memory; and a processing unit adapted to evaluate erase performance of said first block of memory during the first erase cycle therefor and to evaluate erase performance of said second block of memory during the first erase cycle therefor, said processing unit being further adapted to establish and store the initial erase pulse voltage level of the erase pulse applied to said first block of memory based at least in part on the evaluated erase performance of said first block of memory, and said processing unit being further adapted to establish and store the initial erase pulse voltage level of the erase pulse applied to said second block of memory based at least in part on the evaluated erase performance of said second block of memory.

The prior art references must teach or suggest all of the claim limitations. None of the references, however, teach or suggest a first memory location uniquely associated with said first block of memory, said first memory location being adapted to store an initial erase pulse voltage level for an erase pulse to be applied to said first block of memory during the second erase cycle, and said first memory location being adapted to store a first voltage increment threshold count and a second voltage increment threshold count associated with said first block of memory or a second memory location uniquely associated with said second block of memory, said second memory location being adapted to store an initial erase pulse voltage level for an erase pulse to be applied to said second block of memory during the second erase cycle, and said second memory location being adapted to store a first voltage increment threshold count and a second voltage increment threshold count associated with said second block of memory. Therefore, neither Harari '615 nor Harari '148, separately or in combination, teach or disclose all of the elements of claim 17.

Claims 18-20

Claims 18-20 variously depend from claim 17 and are believed to be allowable due at least to their dependency.

II. Fees

Applicants file this Response within three months of the June 7, 2006 Office Action and

with no additional claims. Accordingly, Applicants believe that no extension or claims fees are due. The Commissioner is authorized, however, to charge any fees that may be required, or credit any overpayment, to Deposit Account No. 20-1507.

III. Conclusion

The foregoing is believed to be a complete response to the non-final Office Action mailed June 7, 2006. Applicants respectfully assert that Claims 1-3, 5-8, and 17-24 are in condition for allowance and respectfully request passing of this case in due course of patent office business. If the Examiner believes there are other issues that can be resolved by a telephone interview, or there are any informalities remaining in the application which may be corrected by an Examiner's amendment, a telephone call to Jeff Waters at (404) 885-3082 is respectfully requested.

Respectfully submitted,
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